Electronic Version
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# Claims

[c1] 1.An integrated circuit, comprising:
a)at least one shift register latch, comprising:
i)a first latch;
ii)a second latch in electrical communication with said first latch;
iii)an input for receiving a first clock signal; and
iv)a circuit, connected between said input and said first latch, configured for generating a second clock signal that compensates for any delay in said first clock signal.

[c2] 2.An integrated circuit according to claim 1, further comprising a scan clock tree electrically connected to said input.

[c3] 3.An integrated circuit according to claim 1, wherein said circuit comprises a pulse generator for generating a first clock pulse for said first latch.

[c4] 4.An integrated circuit according to claim 3, wherein said pulse generator comprises an AND gate and an inverter.

[c5] 5.An integrated circuit according to claim 1, wherein said first clock signal comprises a plurality of first pulses each having a first duration and said second clock signal

comprises a plurality of second pulses each having a second duration shorter than said first duration.

[c6] 6.An integrated circuit according to claim 5, wherein each of said plurality of second pulses is generated substantially simultaneously with a corresponding one of said plurality of first pulses.

[c7] 7.An integrated circuit, comprising:
a)a first clock tree for receiving a first clock signal having a plurality of pulses each having a first width; and
b)at least one first shift register latch, comprising:
i)a master latch;
ii)a slave latch in electrical communication with said master latch; and
iii)a circuit element, electrically connected between said first clock tree and said master latch, adapted for generating a second clock signal as a function of said first clock signal.

[c8] 8.An integrated circuit according to claim 7, wherein said circuit element is an AND gate.

[c9] 9.An integrated circuit according to claim 8, wherein said AND gate has a first input for receiving said first clock signal, a second input for receiving a third clock signal that is substantially the inverse of said first clock signal

and a first output in electrical communication with said master latch, said first output for outputting said second clock signal.

[c10] 10.An integrated circuit according to claim 7, further comprising a multiplexer in electrical communication with said master latch.

[c11] 11.An integrated circuit according to claim 7, comprising at least one first scan chain comprising a plurality of first shift register latches.

[c12] 12.An integrated circuit according to claim 11, further comprising at least one second scan chain comprising a plurality of second shift register latches, each of said plurality of second shift register latches lacking said circuit element.

[c13] 13.An integrated circuit according to claim 7, wherein said first clock tree is an LSSD scan clock tree.

[c14] 14.A device, comprising,

a)a power supply,

b)an integrated circuit electrically connected to said power supply, said integrated circuit including at least one shift register latch comprising:

i)a first latch;

ii)a second latch in electrical communication with said

first latch;

iii)an input for receiving a first clock signal; and

iv)a circuit, connected between said input and said first latch, configured for generating a second clock signal that compensates for any delay in said first clock signal.

[c15] 15. A device according to claim 14, further comprising a scan clock tree electrically connected to said input.

[c16] 16.A device according to claim 14, wherein said circuit comprises a pulse generator for generating a first clock pulse for said first latch.

[c17] 17.A device according to claim 16, wherein said pulse generator comprises an AND gate and an inverter.

[c18] 18.A device according to claim 14, wherein said first clock signal comprises a plurality of first pulses each having a first duration and said second clock signal comprises a plurality of second pulses each having a second duration shorter than said first duration.

[c19] 19.A device according to claim 18, wherein each of said plurality of second pulses is generated substantially si-multaneously with a corresponding one of said plurality of first pulses.

[c20] 20.A device according to claim 14, wherein said at least

one shift register latch further comprises a multiplexer in electrical communication with said first latch.